REMARKS

Claims 1-24 are pending in the application and stand rejected.

Claims 1-13 stand provisionally rejected under statutory type (35 U.S.C. § 101) double patenting based on claims 1-13 of a copending, commonly assigned patent application Serial No. 10/455,600. In response, claims 1-13 have been canceled without prejudice, and thus the provisional rejection under 35 U.S.C. §101 is moot.

Claims 14-24 stand provisionally rejected under the judicially created non-statutory, obviousness-type double patenting, based on claims 1-13 of the copending, commonly assigned patent application Serial No. 10/455,600. Applicant respectfully traverses the rejection and respectfully submits that at the very minimum, the claims 1-13 of Serial No. 10/455,600 do not render obvious claim 14 of the present invention.

Claim 14 recites a method of forming a semiconductor device comprising:

(a) forming isolation layers in predetermined regions of a semiconductor substrate to define a first region, a second region and a third region;

(b) forming a first gate insulating layer and a first gate conductive pattern stacked sequentially on the first region, a second gate insulating layer and a second gate conductive pattern stacked sequentially on the second region, and a third gate insulating layer and the second gate conductive pattern stacked sequentially on the third region; and

(c) patterning together the first gate conductive pattern and the second gate conductive pattern to form a first gate electrode, a second gate electrode and a third gate electrode in the first, second and third regions, respectively,

wherein the first gate insulating layer, the second gate insulating layer and the third insulating layer are formed having varying thicknesses and each layer has a different thickness than the other layers.

To support the provisional double patenting rejection, Examiner contends that "it would have been obvious to one of ordinary skill in the art … to isolate each regions by forming isolation regions/layers in the substrate to define a first region, second region, and third region." Even assuming, *arguendo*, that this contention is valid, the Examiner has failed to address other distinct elements of claim 14 which are not recited in claims 1-13 of the pending application Serial No. 10/455,600.

For instance, the Examiner has not addressed other elements of current claim 14 such as "*third gate insulating layer*", "*third gate electrode*", *third gate insulating layer and the second gate conductive pattern stacked sequentially on the third region*", among other features, nor explained how these elements are rendered obvious by claims 1-13 of Serial No. 10/455,600. However, Applicant submits that these features are not disclosed or suggested by claims 1-13 of Serial No. 10/455,600.

Under such circumstances, it is respectfully submitted that Examiner has not met his burden of establishing a *prima facie* case of obviousness-type double patenting against claims 14-24 of the current application. Thus, a terminal disclaimer is not necessary. Accordingly, withdrawal of the provisional rejections is requested.

Respectfully submitted,

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